

09753266-122900

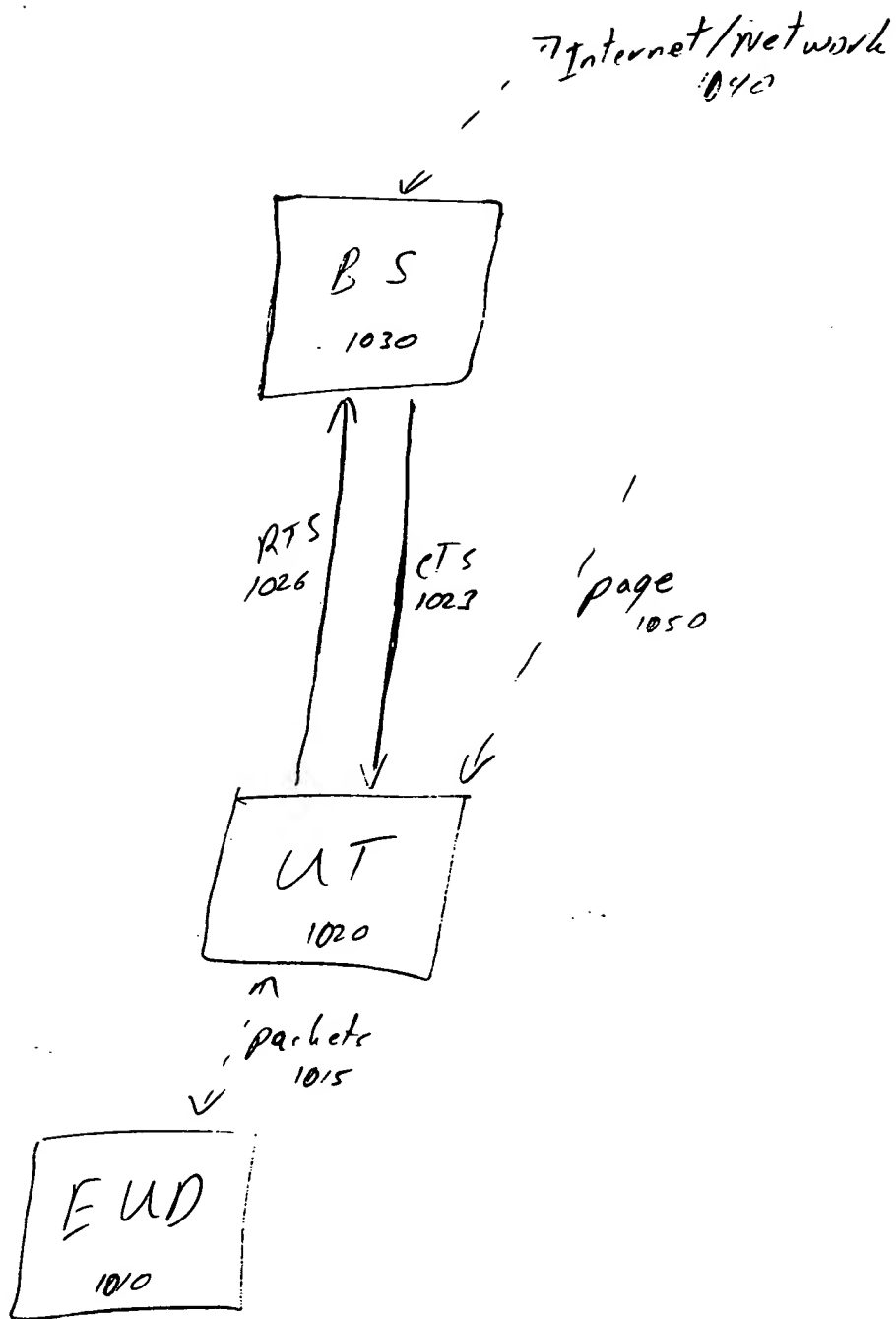


Fig. 1A

	A	B	C
1			
3			
5			
7			
9			
11			
13			
15			

Fig. 1B

09753266-122900

Request Uplink 1310

1310

Receive Uplink Channel — 1320

1320

Receive
Additional
Channels

1330

Request
Additional
Channels

-13%

Receive
Additional
Channels

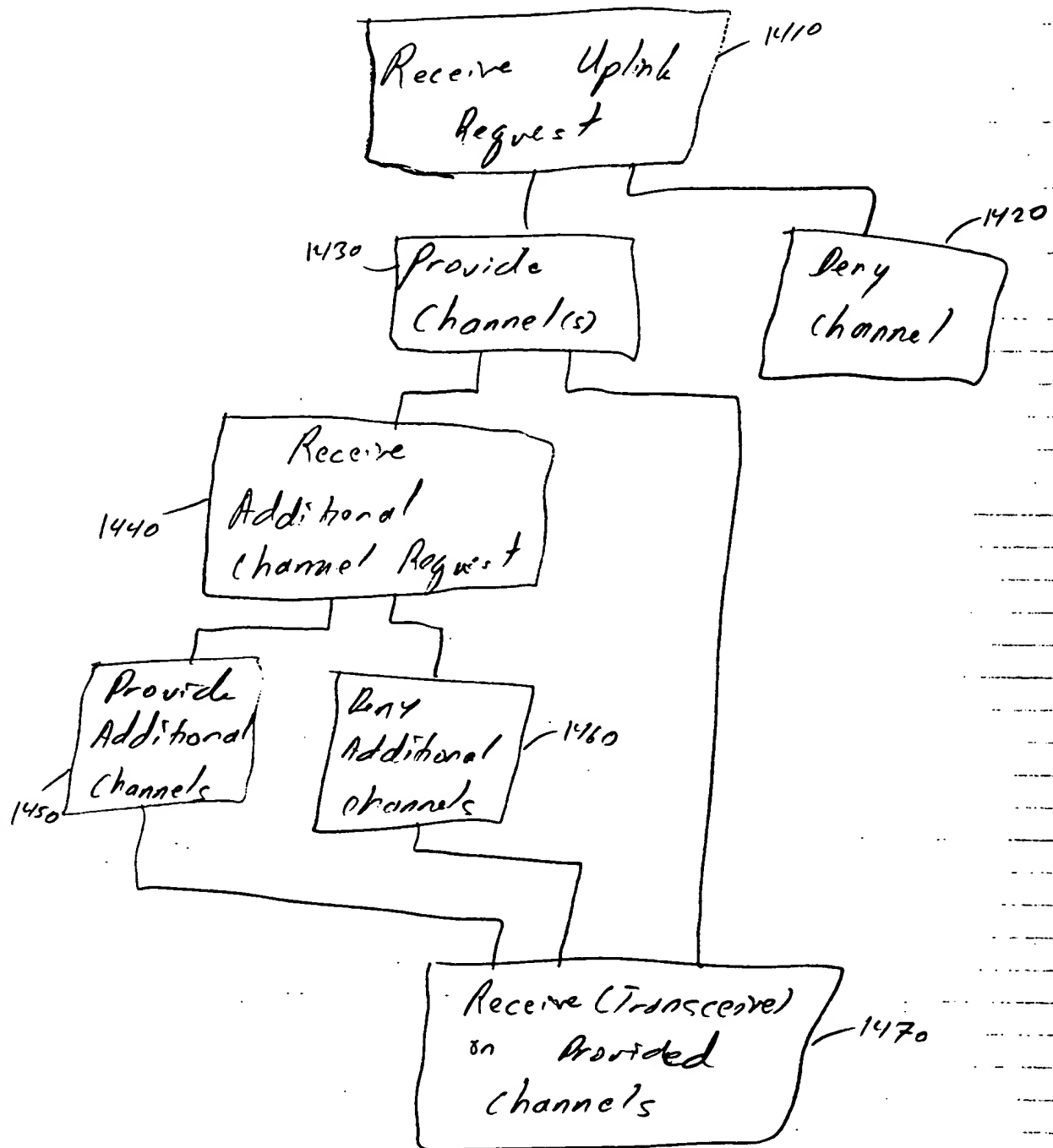
B.50

Transmit (Transceive)
on channels — 1360

-1368

F. 5. 2

Tops
35500



005221 9925250

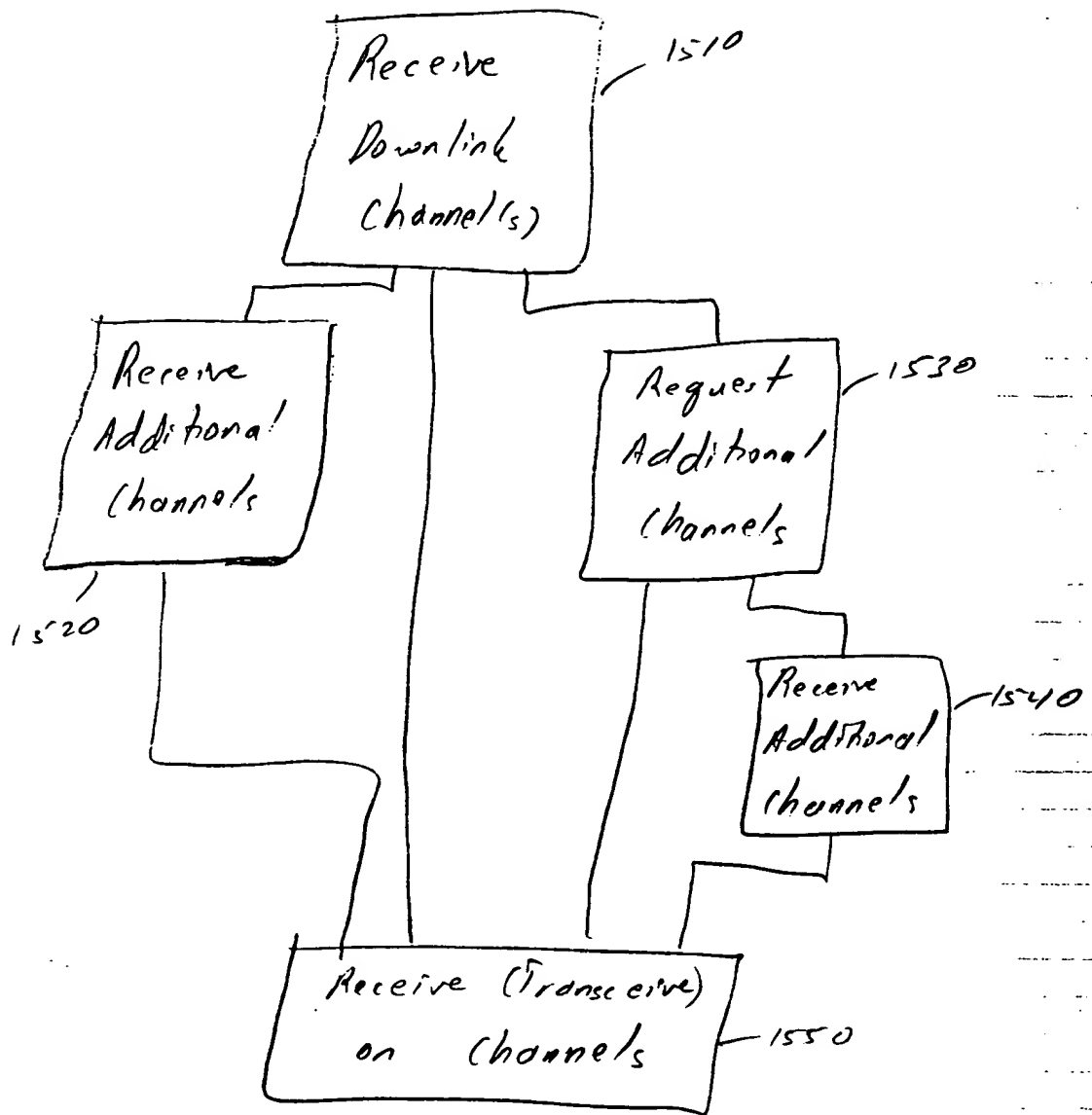
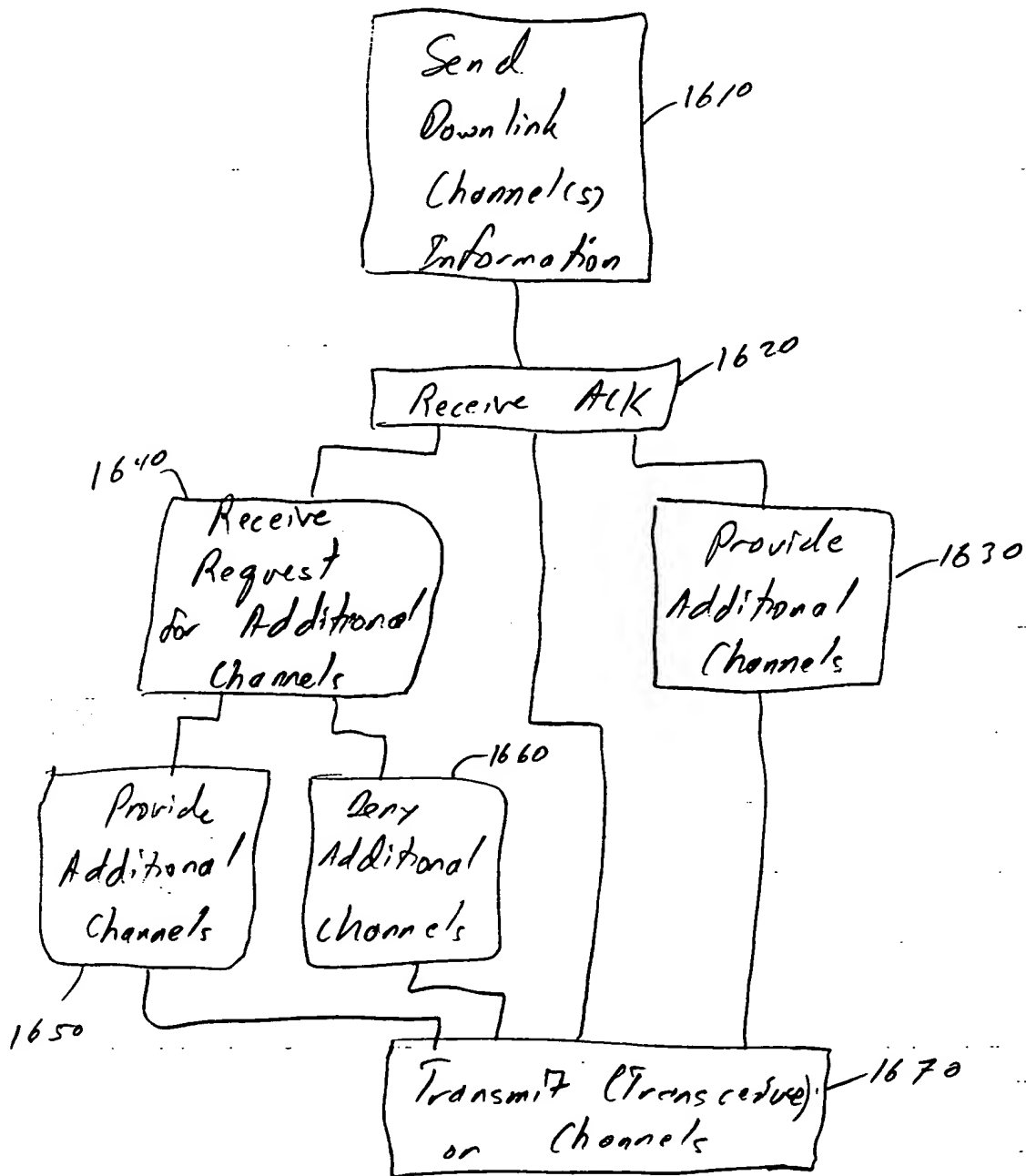


Fig. 4

07423
23522



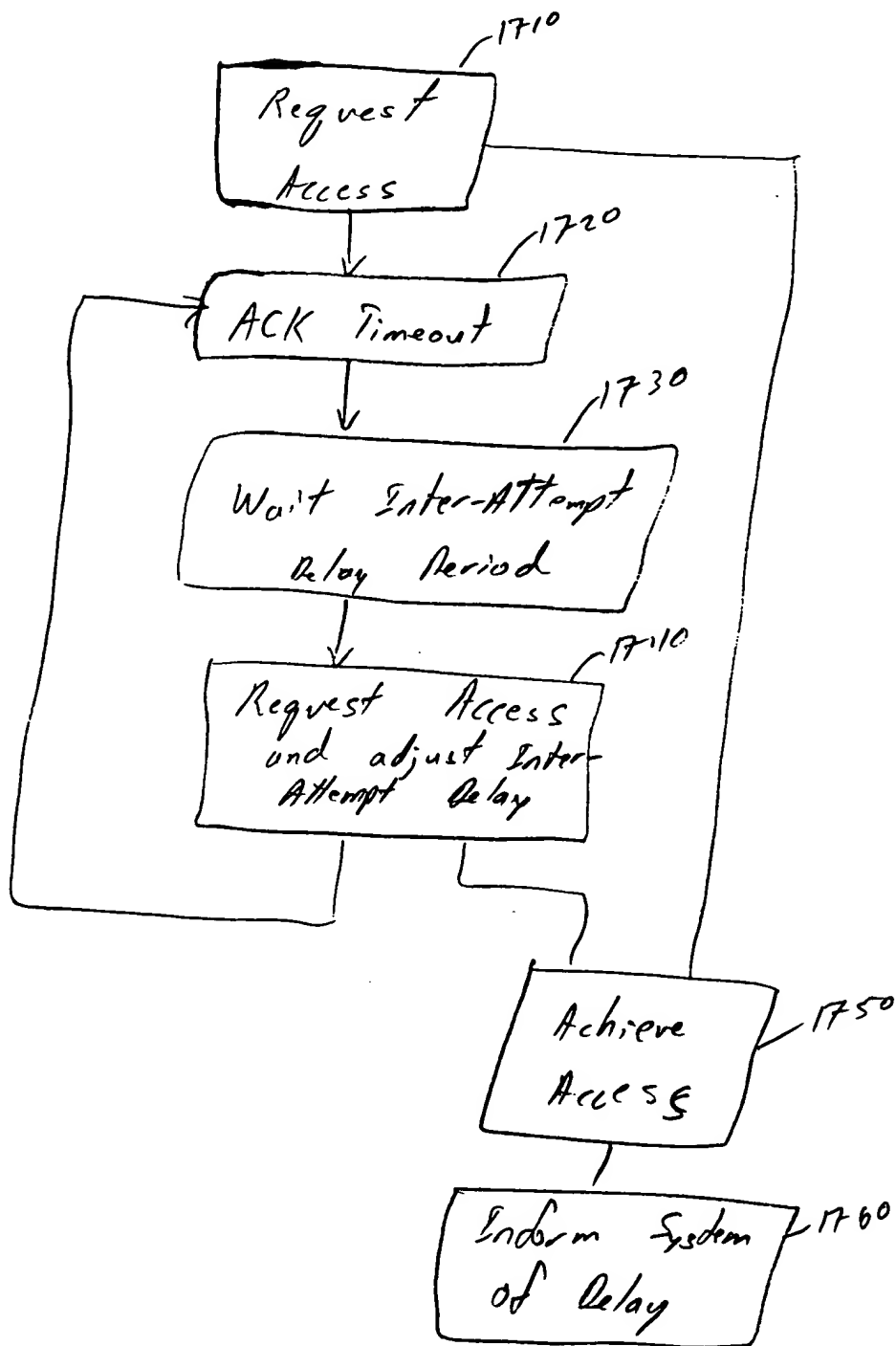


Fig. 6

09753266-123900

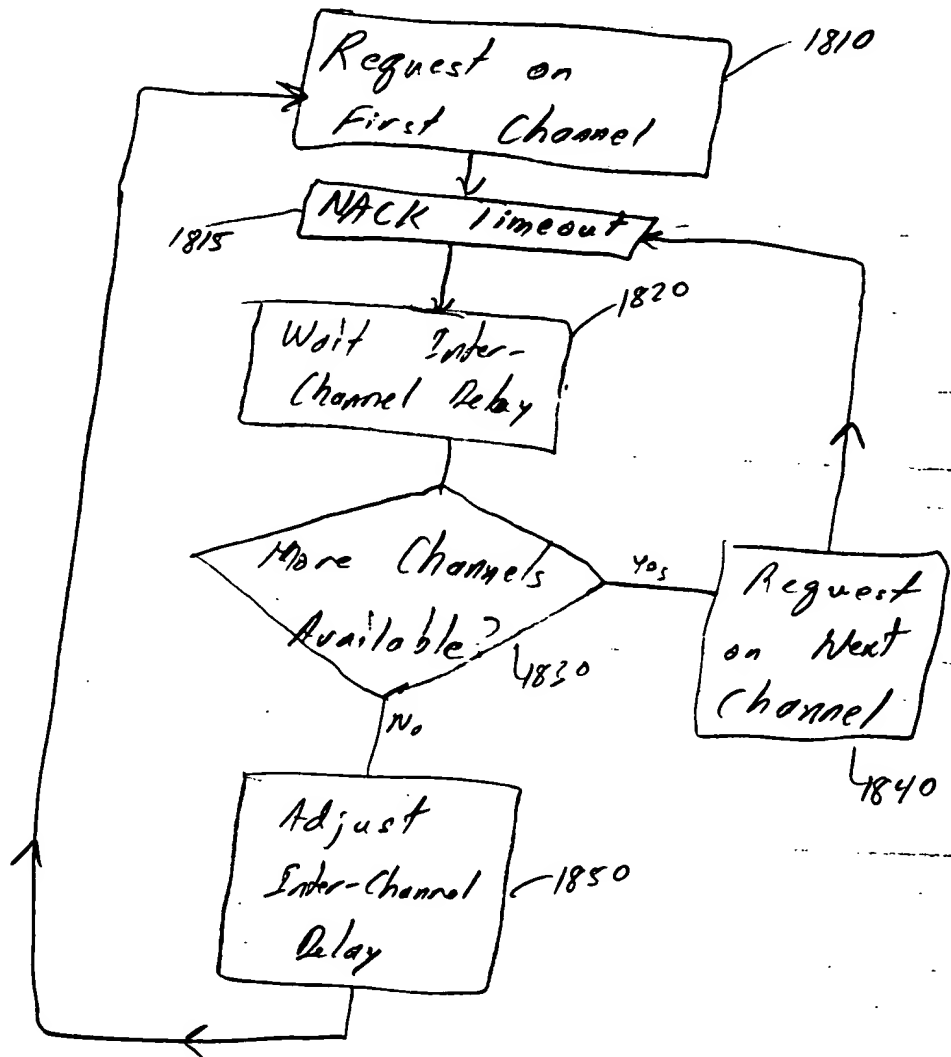


Fig. 7

09753266-122900

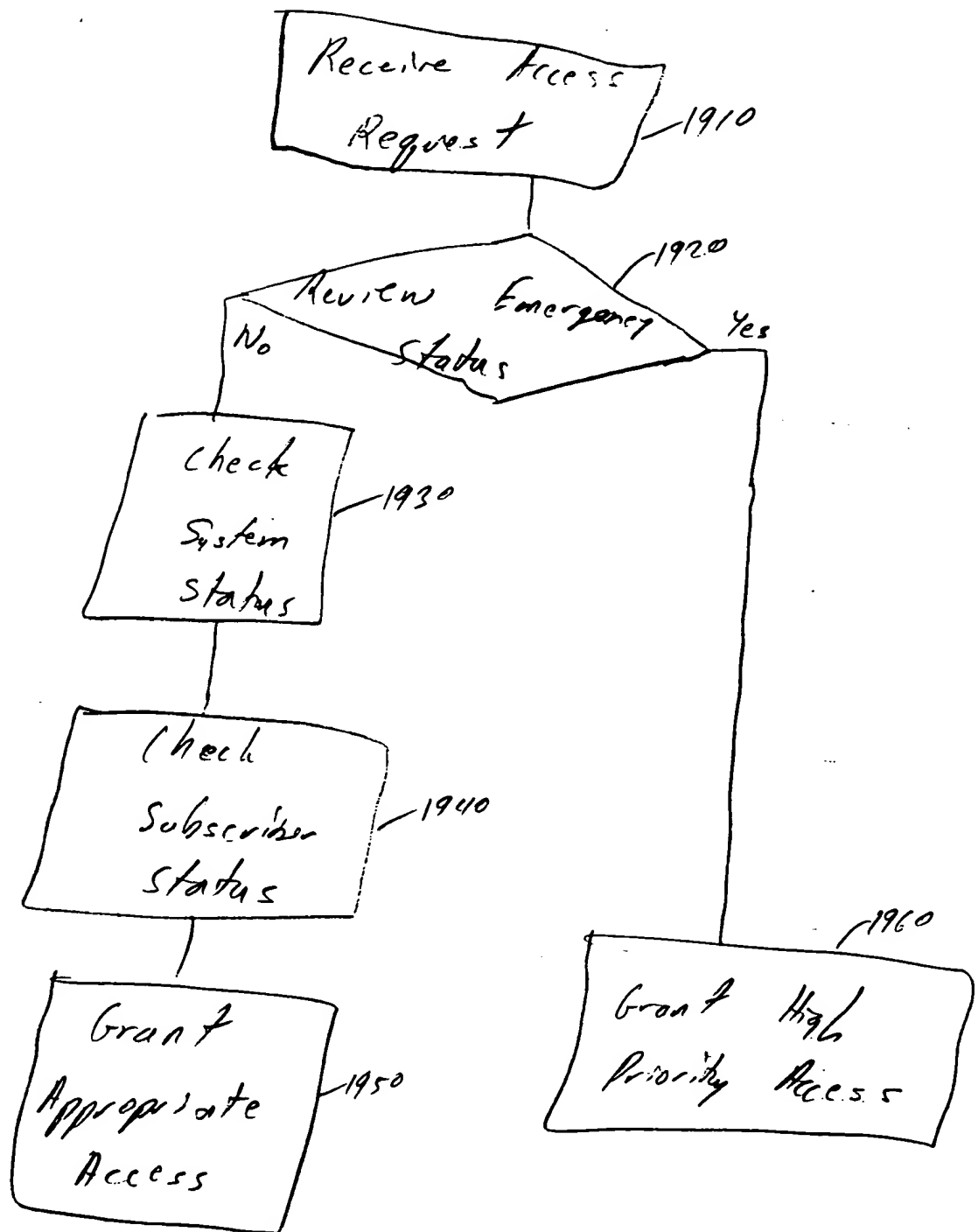


Fig. 8

0053266-12500

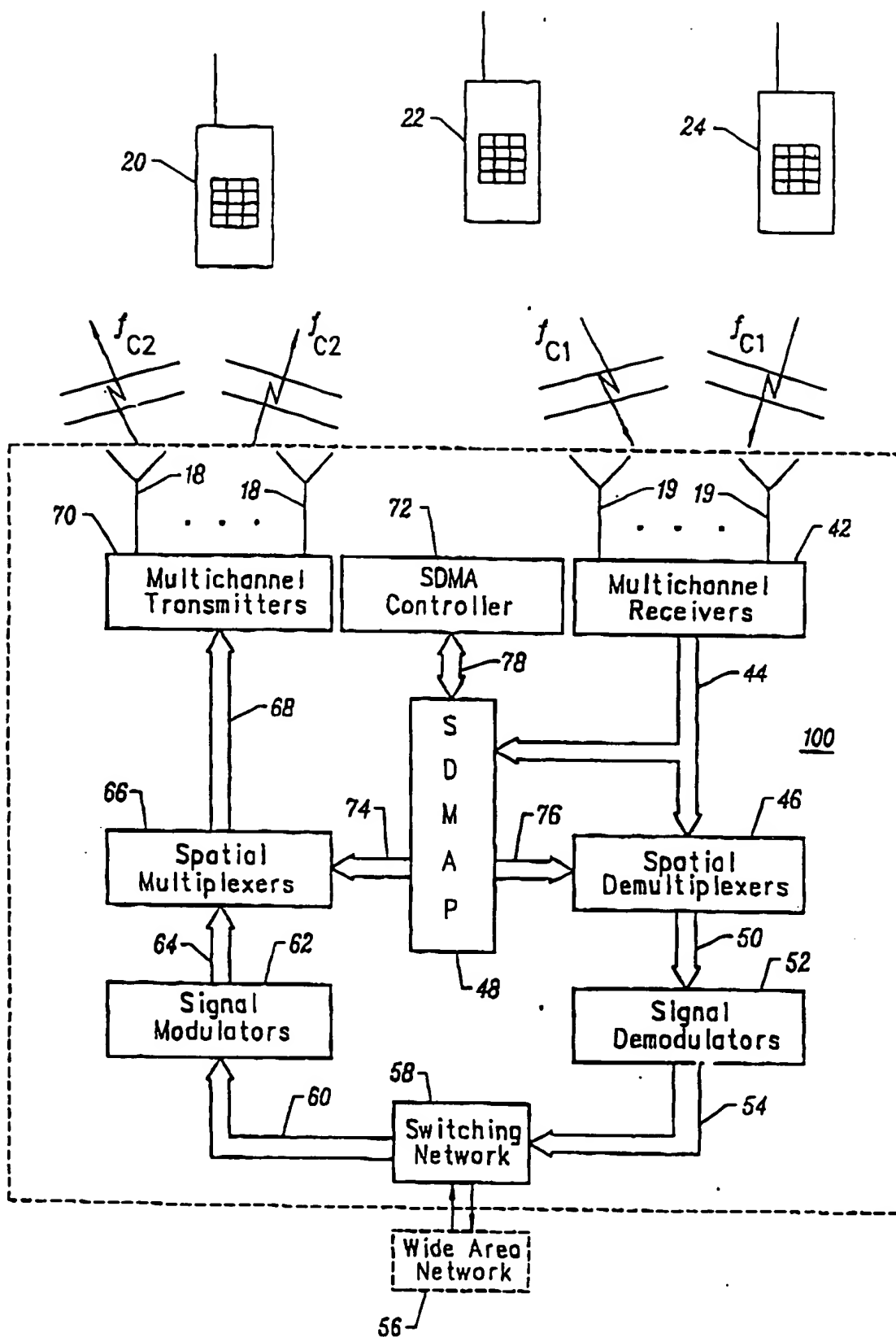


FIG. 9

The diagram illustrates a system architecture for a multi-antenna transmitter. At the bottom, an input labeled "From Signal Modulators" (64) feeds into a block labeled "Spatial Multiplexers" (66). The output of the Spatial Multiplexers (68) is sent to a block labeled "Multichannel Transmitters" (70). The Multichannel Transmitters (70) are connected to three separate antenna arrays (20, 22, 24) at the top. The antenna arrays (20, 22, 24) are shown as rectangular blocks with a grid of elements. The Multichannel Transmitters (70) also have a feedback path (74) connected to a block labeled "SDMA" (48). The SDMA block (48) is a large vertical rectangle containing the letters "S", "D", "M", "A", and "P" stacked vertically. The SDMA block (48) also has a feedback path (74) connected to the Spatial Multiplexers (66). The Multichannel Transmitters (70) are shown with multiple antenna elements (70) and are connected to the antenna arrays (20, 22, 24) via a series of lines (70).

FIG. 10

006321 9925460

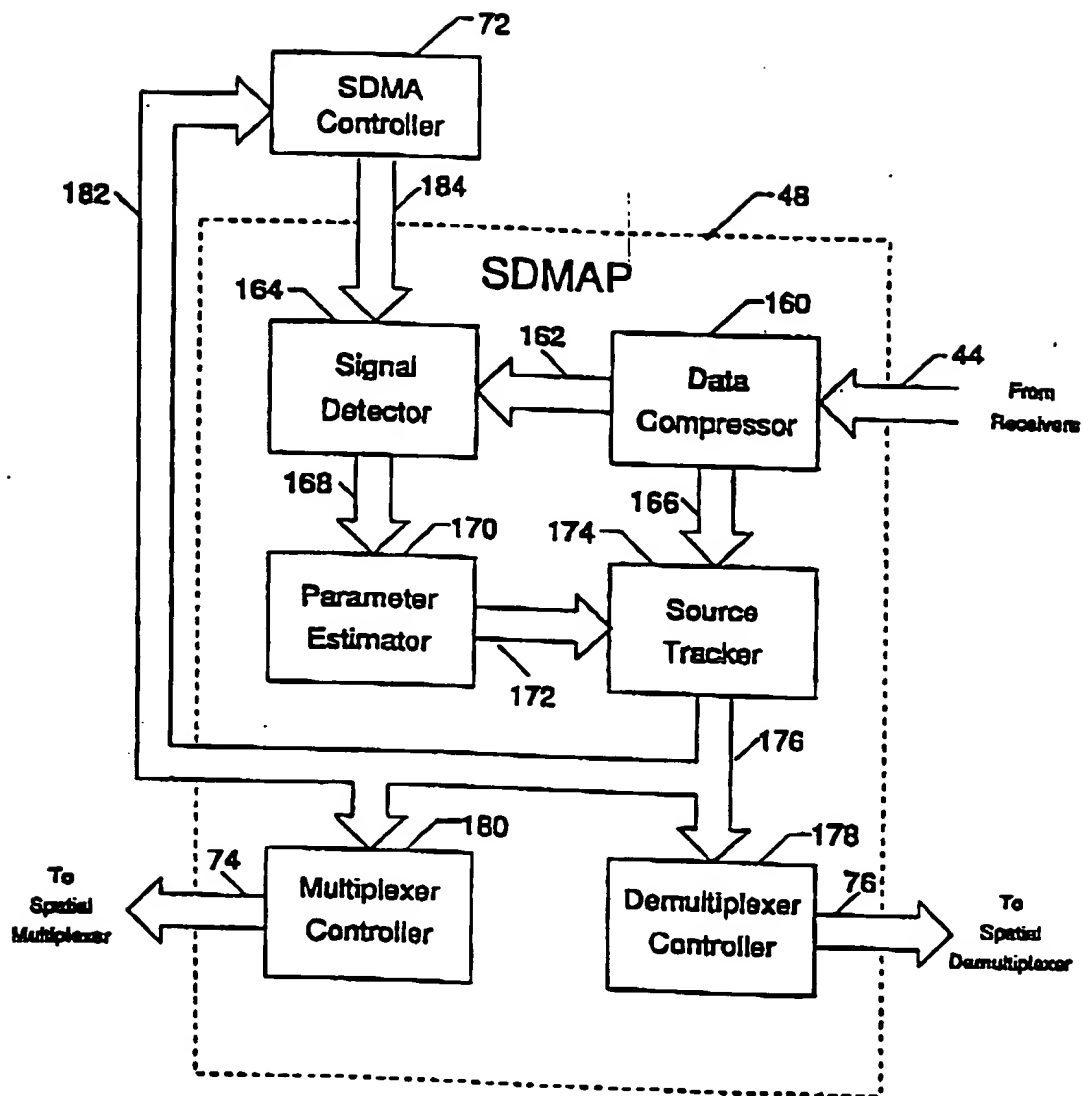


FIG. 1

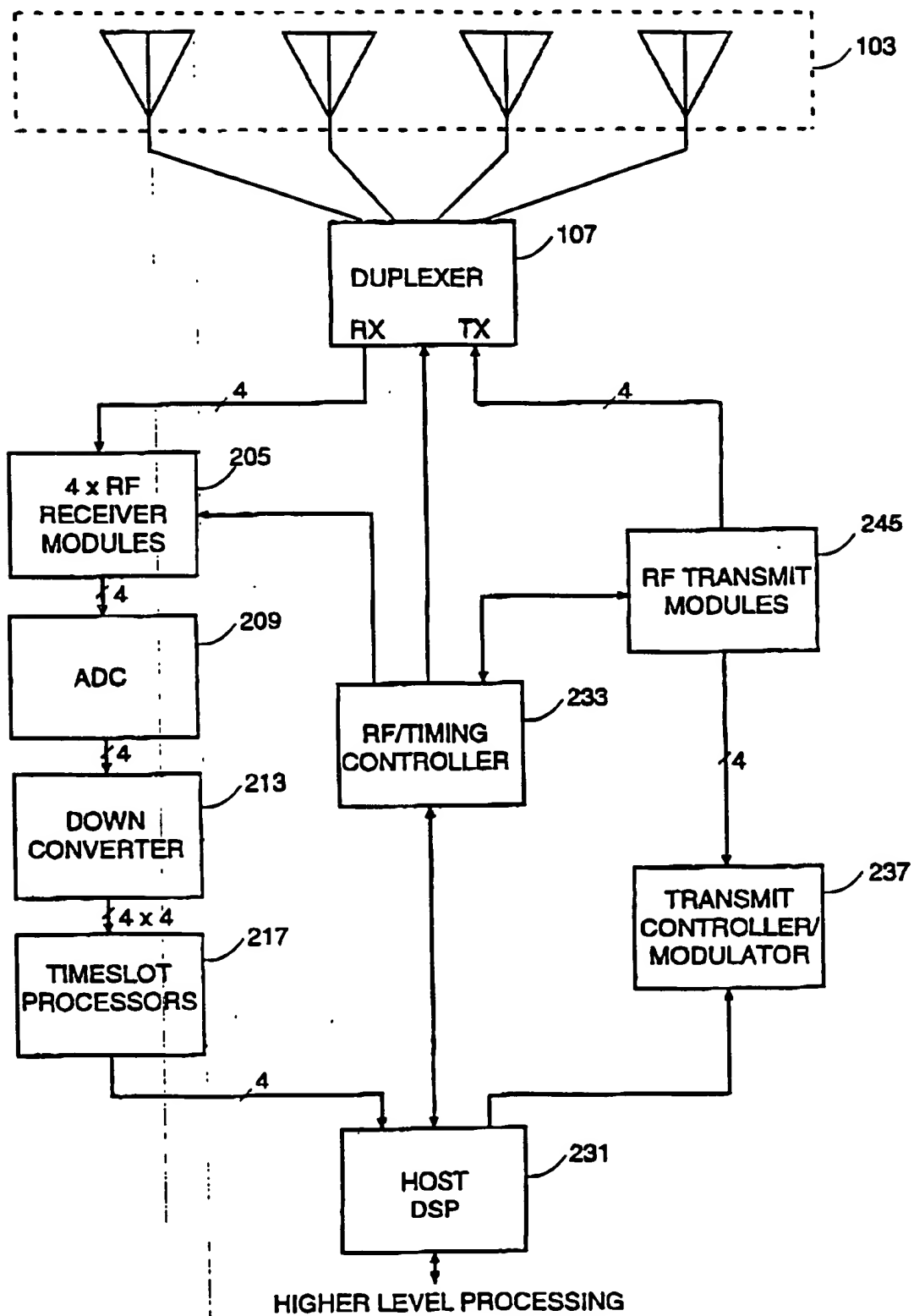


Figure 12

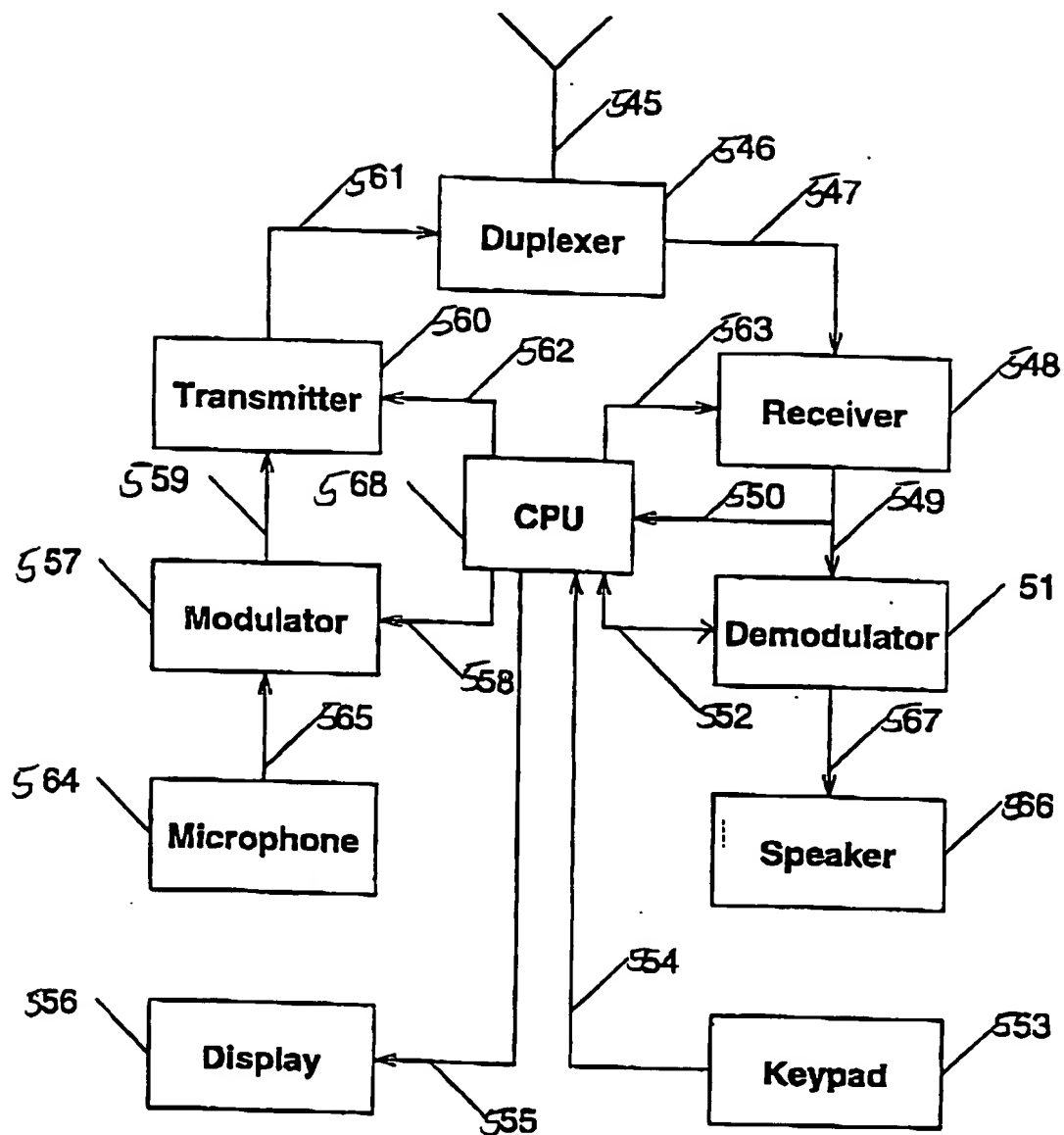


FIG. 13

Timing diagram for the burst structure of the proposed system. The diagram shows a sequence of events over a total duration of 1090 μs . The events are: Ramp-Up (10 μs), Frequency Correction Training (272 μs), Timing Correction Training (256 μs), BCH Preamble (16 μs), Broadcast (BCH) Information (512 μs), Ramp-Down (10 μs), and Interburst Guard (14 μs).

Timing diagram for the APR Burst. The diagram shows a horizontal timeline with segments: Ramp-Up (10 μ s), Training Sequence (260 μ s), Payload (164 μ s), Ramp-Down (10 μ s), Extra Guard Time (86 μ s), and Interburst Guard Time (15 μ s). The total duration is 545 μ s.

Fig. 15

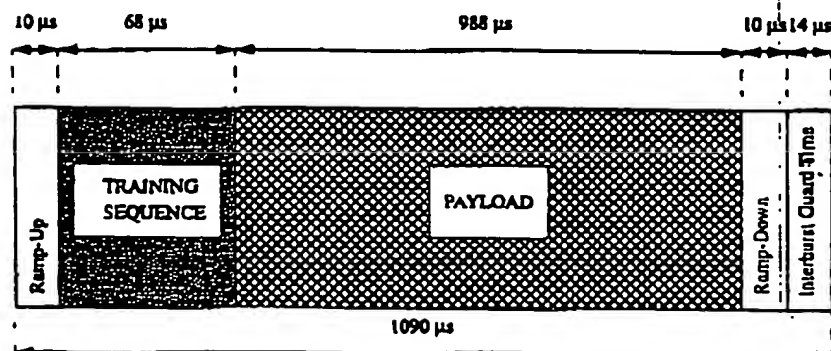


Fig. 16

	Base Station		Remote Terminal
300	Acquire GPS Timing		
302	Determine BCH slot time		
304		BCH \Rightarrow	
306			Scan BCH channels
308			Acquire Frame Timing
310			Acquire Synchronization
312			Build Map of Base Stations BCHs and BSCCs
314			Select Base Station
316			Build CR using UTID and transmit power
318			Scramble CR using BSCC
320		\Leftarrow Configuration Request	
322	Unscramble CR using BSCC		
324	Determine Spatial Signature of Remote CR		
326		Configuration Message \Rightarrow	
328			Adjust timing and power
330		\Leftarrow Traffic Request	
332		Traffic Assignment \Rightarrow	
334		\Leftarrow Traffic \Rightarrow	
336		Send packet \Rightarrow	
338		\Leftarrow Send DA and packet	
340		Send DA and packet \Rightarrow	
342		\Leftarrow Send DA and packet	

Figure 17